

Figure 1 is a block diagram of a multi-processor system 10. The system includes three identical processing units (18a, 18b, 18c) connected to a common bus 32. Each unit contains a Processor, a debug interface, and a logic block (14a, 14b, 14c). The logic blocks are connected to the bus via multiplexers (20a, 20b, 20c) and control signals (12a, 12b, 12c). The debug interfaces are connected to the processors via control signals (15a, 15b, 15c).

FIG. 1

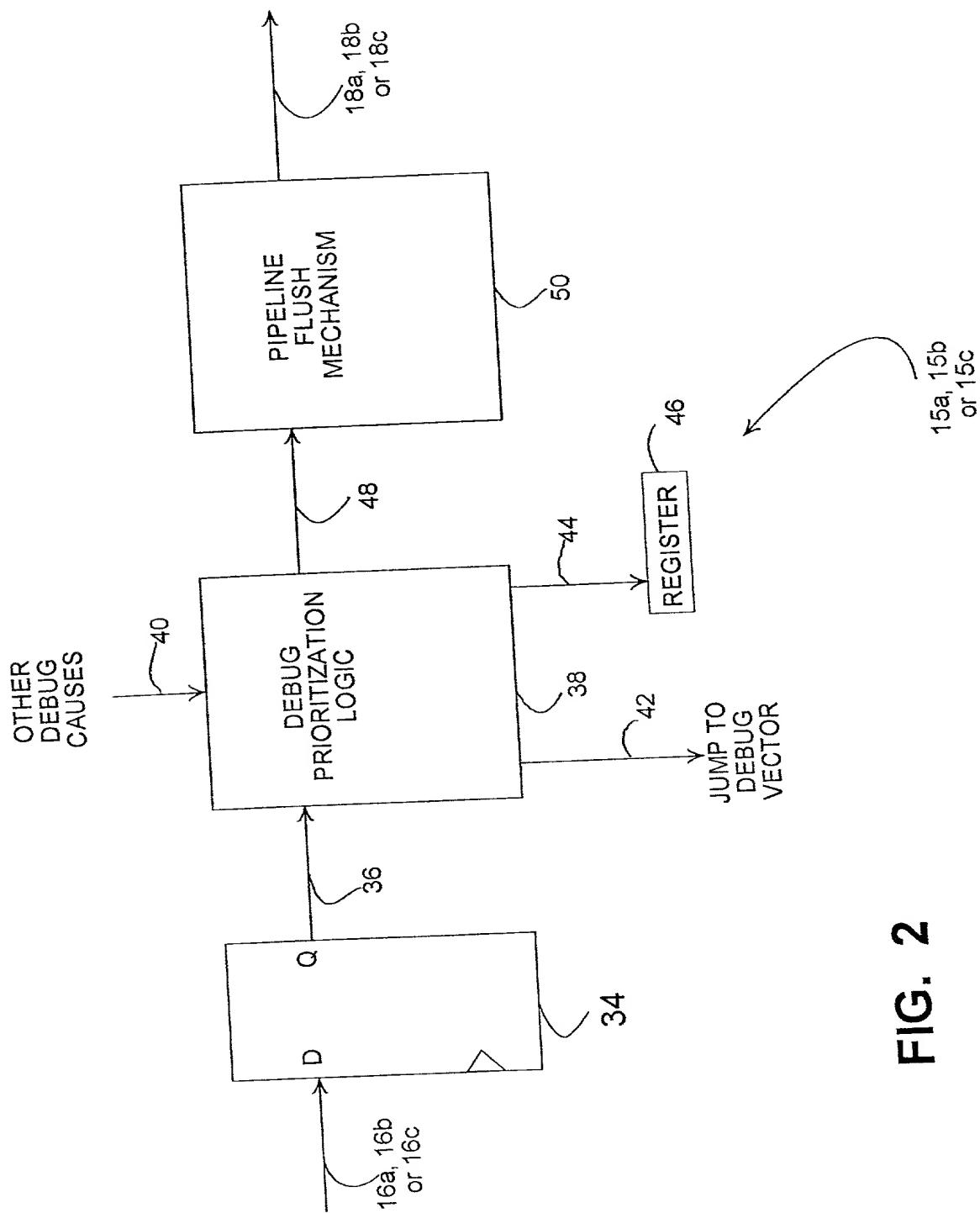


FIG. 2